



#9/B  
5/15/03  
PATENT  
51270-277019  
Adm H

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

TSUJI et al.

Serial No: 09/982,335

Filed: October 18, 2001

For: SEMICONDUCTOR INPUT  
PROTECTION CIRCUIT

Art Unit: 2811

Examiner: NADAV, ORI

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents Washington D.C. 20231, on

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AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated January 6, 2003 in connection with the above-identified application the period of response extended by one month, to May 6, 2003, by the attached petition and fee, please enter and consider the following amendment and remarks.

IN THE CLAIMS:

Claims 3, 4, 7, 8, 11, 13, 20, 21, and 22 have been cancelled, without prejudice.

Claims 1 and 5 have been amended. Claims 23 - 26 have been added.

1. (Twice Amended) An input protection circuit comprising: